REMARKS

Prior to this Reply, Claims 1-43 were pending. Through this Reply, Claims 1, 3, 4, 7-10, 12, 15-17, 20-23, 27, 31-33 and 39 have been amended. No claims have been added or cancelled. Accordingly, Claims 1-43 are now at issue in the present case.

I. Rejection of Claims 1-43 Under 35 U.S.C. § 102(e)

The Examiner rejected Claims 1-43 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,523,102 to Dye et al. (hereinafter "Dye"). Applicant respectfully traverses the rejection.

A. Claims 1, 15 and 27

1. Claims 1, 15 and 27 are patentable at least because Dye fails to disclose storing the compressed data in a memory different from the main memory

Claims 1, 15 and 27 (as amended) emphasize that, in the claimed embodiment, the memory where the compressed data is stored is *different from the computing system main memory*. Support can be found at least at Fig. 2 and page 7, lines 12-15 of the present application.

The Examiner asserts that the claimed step of "storing said data in memory" is taught by Dye in the "abstract" and at "col. 85, lines 40-48." With respect to the Abstract, it is noted that Dye teaches that components "of the present invention keep recently used pages compressed *in the system memory*. Additional performance is gained by the transfer of compressed pages between *the system memory* and the disk and network subsystems." (Abstract, lines 23-27, emphasis added). With respect to Col. 85, Dye teaches "writing the first compressed data to a first compressed portion *of the system memory*." (Col. 85, line 46-47, emphasis added).

Accordingly, it is believed Claims 1, 15 and 27, as amended, distinguish over Dye at least because Dye fails to anticipate a method that includes storing the compressed data in a controller memory, which is *different from* the system memory (Claims 1 and 15) or a memory controller with circuitry wherein compressed data is stored in a controller memory which is *different from* the system memory (Claim 27).

2. Claim 15 is further patentable at least because Dye fails to disclose storing the compressed data in memory which is part of a memory controller

Although Dye discloses that a computer system may have a memory controller (e.g., Fig. 1), there is no disclosure that the memory where the compressed data is stored is part of the memory controller. As noted above, citations in Dye refer to a "compressed cache" which is part of the main system memory.

In contrast, Claim 15, as amended, includes writing compressed data to a controller memory, where the memory controller *includes* the controller memory. This is illustrated, e.g., in Fig. 2 of the present application.

Accordingly, it is believed Claim 15, as amended, distinguishes over Dye at least because Dye fails to anticipate a method that includes the step of storing the compressed data in a controller memory, which is *included in* the memory controller.

B. Claim 40

Claim 40 is patentable at least because Dye fails to anticipate:

> after said step of compressing at least a first portion of said second data, writing at least a portion of said second data to memory without compressing said at least a second portion of said second data

The Examiner did not point to any particular portion of Dye as assertedly anticipatory of this portion of Claim 40. It appears, however, that the system of Dye would not operate as

claimed in Claim 40. Rather, it is believed that when Dye receives data at an interface, either all or none of the received data is compressed. For example, as described at Col. 23, line 66 to Col. 24, line 27:

> When the system memory controller 210 writes data to DRAM memory 575, the data is written into the DRAM memory 575 through the damping resistor 589. During this write process the address and control bus 577 from the system memory controller 210 is snooped by the compactor chip 250 and *a determination is made (based on the snooped address) if the data is intended for the compactor chip 250 or the DRAM 575.* If the address is in the active aperture window of the compactor chip 250 the data is written to both the DRAM memory 575 and the compactor chip 250. The transceiver 16245 may be used to electrically de-couple the signals from the DRAM memory data bus 583. In alternate embodiments, the 16245 Transceivers may not be used, as data and addresses may be routed directly between the compactor chip 250 and the DRAM memory 575. During a read of data by the system memory controller 210 from the C-DIMM 550, data is read from the DRAM memory 575 when the address is outside the compactor chip 250 address comparison window, and from the compactor chip 250 when the address is within the address comparison window. In the preferred embodiment, the compactor chip 250 registers some of the DRAM control signals 579. Other registered control and address signals 594 sent by the registers 573 also control the operation of the DRAM 575. *The control and address buses 594 and 579 control which device, compactor chip 250 or DRAM 575 outputs data to the system memory controller 210 through the damping resistor 589 onto the memory bus 587.* (emphasis added)

Thus, it appears that, according to Dye, whether or not to compress data which is sent from the memory controller is done on an all-or-nothing basis (with respect to any particular write request).

Accordingly, it is believed that Claim 40 distinguishes over Dye at least because it is believed Dye fails to anticipate a method that includes "after said step of compressing at least a first portion of said second data, writing at least a portion of said second data to memory *without compressing* said at least a second portion of said second data" (emphasis added).

C. Dependent Claims 2-14, 16-26, 28-39 and 41-43

The dependent claims are patentable at least as dependent, directly or indirectly, from the independent claims, and for other reasons, as well.

Regarding Claims 10 and 23, it is believed Dye fails to disclose *not* compressing data when an attempted compression results in expansion (Claim 23) or is determined to be not compressible (Claim 10).

Claims 2-4, 16, 27-29 and 39-40 were rejected because the Examiner asserts that "Dye, et al. teaches said data is received from said source at a first data rate and stored in said memory at a second data rate wherein said first data rate is greater than said second data rate. [*col. 8, lines 54-65*]"

Col. 8, lines 54-65 reads as follows:

> The present invention includes parallel data compression and decompression logic, designed for the reduction of data bandwidth and storage requirements and for compressing and decompressing data at a high rate. The compression/decompression logic may be referred to as a "Compactor Chip." The Compactor Chip may be included in any of various devices, including, but not limited to: a memory controller; memory modules such as a DIMM; a processor or CPU; peripheral devices, such as a network interface card, modem, IDSN terminal adapter, ATM adapter, etc.; and network devices, such as routers, hubs, switches, bridges, etc., among others.

Applicant believes the language cited by the Examiner does not constitute an anticipation of Claims 2-4, 16, 27-29 and 39-40. There does not appear to be an anticipatory disclosure of relative data rates for receipt and storage in this citation. Accordingly, Applicant respectfully requests withdrawal of the rejection of Claims 2-4, 16, 27-29 and 39-40.

Regarding Claims 41-43, the Examiner asserts that "Dye, et al. teaches a first compression flag to signal that said first data has been compressed [*col. 44, line 48 thru col. 45, line 3*]." Applicant notes that the "compression flag" of Claim 41 is a term indicated, in the specification, as referring to a flag which is "maintained" with respect to each block of data that

is stored into the controller memory, e.g., so that the flag can be used to determine whether or not the data was compressed (page 13, lines 11-15).

In contrast, the Examiner cites a portion of Dye which refers to a "writing flag" and "reading flag . . . to indicate that a compressed cache read is being processed." However, it is clear that the "reading flag" is not the claimed compression flag, because it is not maintained and is not (and, it is believed, could not be) used to determine whether to perform decompression, at a later time. The read and write flags are used to indicate the status of current reading or writing operations, and are cleared as soon as those operations are over.

At Col. 37, lines 43-51, Dye notes:

> When the Creating flag is set, then the cache entry 804 is in the process of being allocated. When the Reading flag is set, then the cache entry 804 is in the process of being reused. When the Writing flag is set, then the cache entry 804 is in the process of being written back to disk. When the Replacing flag is set, then the compressed page associated with the cache entry 804 is in the process of being replaced.

It is believed, from this, that the reading and writing flags of Dye can not be the claimed compression flags, because if they were "maintained," as are compression flags, they could not be used for indicating current status, as desired by Dye.

Regarding Claims 42 and 43, it is believed Dye fails to disclose a peripheral device *channel* as the second interface and fails to disclose performing a CRC operation or providing a parity value, as claimed.

Although the comments above are believed to substantively distinguish the cited reference, Applicant does not necessarily admit that Dye is prior to the present invention. It is believed the above comments establish patentability and Applicant does not necessarily accede in the assertions and statements in the Office Action, whether or not expressly addressed.

II. Additional Claim Fees

In determining whether additional claim fees are due, reference is made to the Fee Calculation Table (below).

Fee Calculation Table

	Claims Remaining After Amendment		Highest Number Previously Paid For	Present Extra	Rate	Additional Fee
Total (37 CFR 1.16(c))	43	Minus	43	= 0	x $18 =	$ 0.00
Independent (37 CFR 1.16(b))	4	Minus	4	= 0	x $86 =	$ 0.00

As set forth in the Fee Calculation Table (above), Applicant previously paid claim fees for forty-three (43) total claims and for four (4) independent claims. Therefore, Applicant believes that no additional claims fees are due. Nevertheless, the Commissioner is hereby authorized to charge Deposit Account No. 50-2198 for any fee deficiencies associated with filing this paper.

III. Conclusion

Applicant believes that the application appears to be in form for allowance. Accordingly, reconsideration and allowance thereof is respectfully requested.

The Examiner is invited to contact the undersigned at the below-listed telephone number regarding any matters relating to the present application.

Respectfully submitted,

Tejpal S. Hansra

Tejpal S. Hansra
Registration No. 38,172
Hansra Patent Services
4525 Glen Meadows Place
Bellingham, WA 98226
(360) 527-1400

Date: Dec. 1, 2003